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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,295	05/29/2001	Hiroyuki Hebiguchi	9281-3980	7331

7590 09/10/2003  
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EXAMINER

LEWIS, DAVID LEE

ART UNIT	PAPER NUMBER
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2673

DATE MAILED: 09/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/870,295

Applicant(s)

HEBIGUCHI, HIROYUKI

Examiner

David L Lewis

Art Unit

2673

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on 23 June 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☐ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

***Claim Rejections - 35 U.S.C. § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

1. **Claims 1-21 are rejected under 35 U.S.C. 102(a) as being anticipated by Negishi et al. (5907314).**

2. **As in claim 1, Negishi et al. teaches** of a liquid crystal display comprising: a pair of substrates which face each other and a liquid crystal held therebetween, **figure 3 item 1**; a plurality of source lines and a plurality of gate lines arranged in a matrix on one of the pair of substrates, **figure 3 item 6, figure 4 items 10, 12, 13**, the plurality of source lines each being divided into two groups in a direction of extension of the source lines, such that at least one of the source lines does not extend across at least one of the gate lines, **figure 4 items 12 and 13**; a first source driver to apply image signals to one group of the divided source lines, **figure 4 item 12**; a second source driver to apply image signals to the other group of the divided source lines, **figure 4 item 13**; a first gate driver to apply scanning signals to the plurality of gate lines that extend across the one group of the divided source lines, **figure 4 item 10 (X1 to XM), figure 11 item 115**; a second gate driver to apply scanning signals to the plurality of gate lines that extend across the other group of the divided source lines, **figure 4 item 10 (XM+1 to XN), figure 11 item 116**; and a switching unit to switch and allocate an image signal from

each of the first and second source drivers to a predetermined number of the source lines, **figure 5**.

3. **As in claim 10, Negishi et al. teaches** a method of increasing ease of writing in a liquid crystal display, the method comprising: selecting two sets of image signals, each image signal selected from a plurality of image signals, **figure 5 items Sv and Sv1**; applying each set of image signals to one of two groups of divided source lines, **figure 4 items 12 and 13**; and applying scanning signals to two groups of gate lines, each group of gate lines extending across a corresponding group of the divided source lines such that at least one of the source lines does not extend across at least one of the gate lines, **figure 4 item 10, figure 11 item 110, figure 12 item 130**.

4. **As in claim 19, Negishi et al. teaches of** a liquid crystal display comprising: a pair of substrates which face each other and a liquid crystal held there between, **figure 10**; a plurality of source lines and a plurality of gate lines arranged in a matrix, the plurality of source lines being divided into two groups in a direction of extension of the source lines, such that at least one of the source lines in each group does not extend across at least one of the gate lines, **figure 11 items 112 and 113**; a first source driver to apply image signals to one group of the divided source lines, **figure 11 items 112**; a second source driver to apply image signals to the other group of the divided source lines, **figure 11 items 113**; a first gate driver to apply scanning signals to the plurality of gate lines that extend across the one group of the divided source lines, **figure 11 item 115**; a second gate driver to apply scanning signals to the plurality of gate lines that

extend across the other group of the divided source lines, **figure 11 item 116**; and a switching unit to switch and allocate an image signal from each of the first and second source drivers to a predetermined number of the source lines, **figure 12 item 109**.

5. As in claim 2, Negishi et al. teaches wherein the predetermined number of source lines is two to four, figure 4 item Y1 to YN. As in claim 3, Negishi et al. teaches wherein the predetermined number of source lines is three, figure 4 item Y1 to YN. As in claim 4, Negishi et al. teaches wherein image signals having inverse polarities are output from adjacent outputs of the first and second source drivers, column 12 lines 3-22, column 17 lines 40-45. As in claim 5, Negishi et al. teaches wherein image signals having inverse polarities are output from opposing outputs of the first and second source drivers, column 12 lines 3-22, column 17 lines 40-45. As in claim 6, Negishi et al. teaches wherein scanning signals are applied substantially symmetrically by each gate driver, figure 18, column 18 lines 40-67, column 29 lines 40-51. As in claim 7, Negishi et al. teaches wherein the first gate driver applies scanning signals starting from a gate line most proximate to the first source driver and proceeding towards a gate line most distal to the first gate driver, figure 16 items 110a. As in claim 8, Negishi et al. teaches wherein the second gate driver applies scanning signals starting from a gate line most proximate to the second source driver and proceeding towards a gate line most distal to the second gate driver, figure 16 items 110b. As in claim 9, Negishi et al. teaches wherein each scanning signal applied by the first gate driver is substantially simultaneous with the symmetric scanning signal applied by the second gate driver, figure 12 item 130, figure 16 items 110a and 110b.

6. As in claim 11, Negishi et al. teaches wherein the selecting comprising demultiplexing each image signal from the plurality of image signals, figure 14. As in claim 12, Negishi et al. teaches wherein further comprising dividing the source lines into two groups of source lines and the gate lines into two groups gate lines, figure 11 items 112, 113, 115, and 116. As in claim 13, Negishi et al. teaches wherein further comprising inverting polarities of adjacent image signals of each of the two groups of image signals, column 12 lines 3-22, column 17 lines 40-45. As in claim 14, Negishi et al. teaches wherein further comprising applying one scanning signal to one of the two groups of gate lines substantially simultaneously with applying one scanning signal to the other of the two groups of gate lines, column 26 lines 28-38. As in claim 15, Negishi et al. teaches wherein further comprising applying the scanning signals substantially symmetrically between the two groups of gate lines, column 12 lines 3-22, column 17 lines 40-45, column 26 lines 28-38. As in claim 16, Negishi et al. teaches wherein further comprising applying the scanning signals to the two groups of gate lines such that the substantially simultaneously applied scanning signals progressively approach each other, figure 12 item 130, figure 16 items 110a and 110b. As in claim 17, Negishi et al. teaches wherein further comprising applying the scanning signals to the two groups of gate lines such that the substantially simultaneously applied scanning signals remain the same distance from each other, figure 12 item 130, figure 16 items 110a and 110b. As in claim 18, Negishi et al. teaches wherein further comprising balancing a writing time of the image signals on the selected source lines with a capacitance formed at areas of overlap of the source lines and gate lines to provide a desired increase in ease of writing, figure 11 item 105. As in claim 20, Negishi et al. teaches of liquid crystal display according to claim 19, wherein scanning signals are applied substantially symmetrically by each gate driver, figure 12 item 130, figure 16 items 110a, 110b, figure

18, column 30 lines 5-40. As in claim 21, Negishi et al. teaches of liquid crystal display according to claim 1, wherein the plurality of gate lines that extend across the one group of the divided source lines do not extend across the other group of the divided source lines, figure 11 items 115 and 116.

### ***Response to Arguments***

7. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection. See the new rejection over Negishi et al., figures 4 and 11.

### ***Conclusion***

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

9. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. **6369791, 6124853, 5852428, 6094243.**
11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L Lewis whose telephone number is 703 306-3026. The examiner can normally be reached on M, T, TH, F.
12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703 305-4938.
13. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-4700.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks  
Washington, D.C. 20231

**or faxed to:**


(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

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September 7, 2003

  
BIPIN SHALWALA  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600